

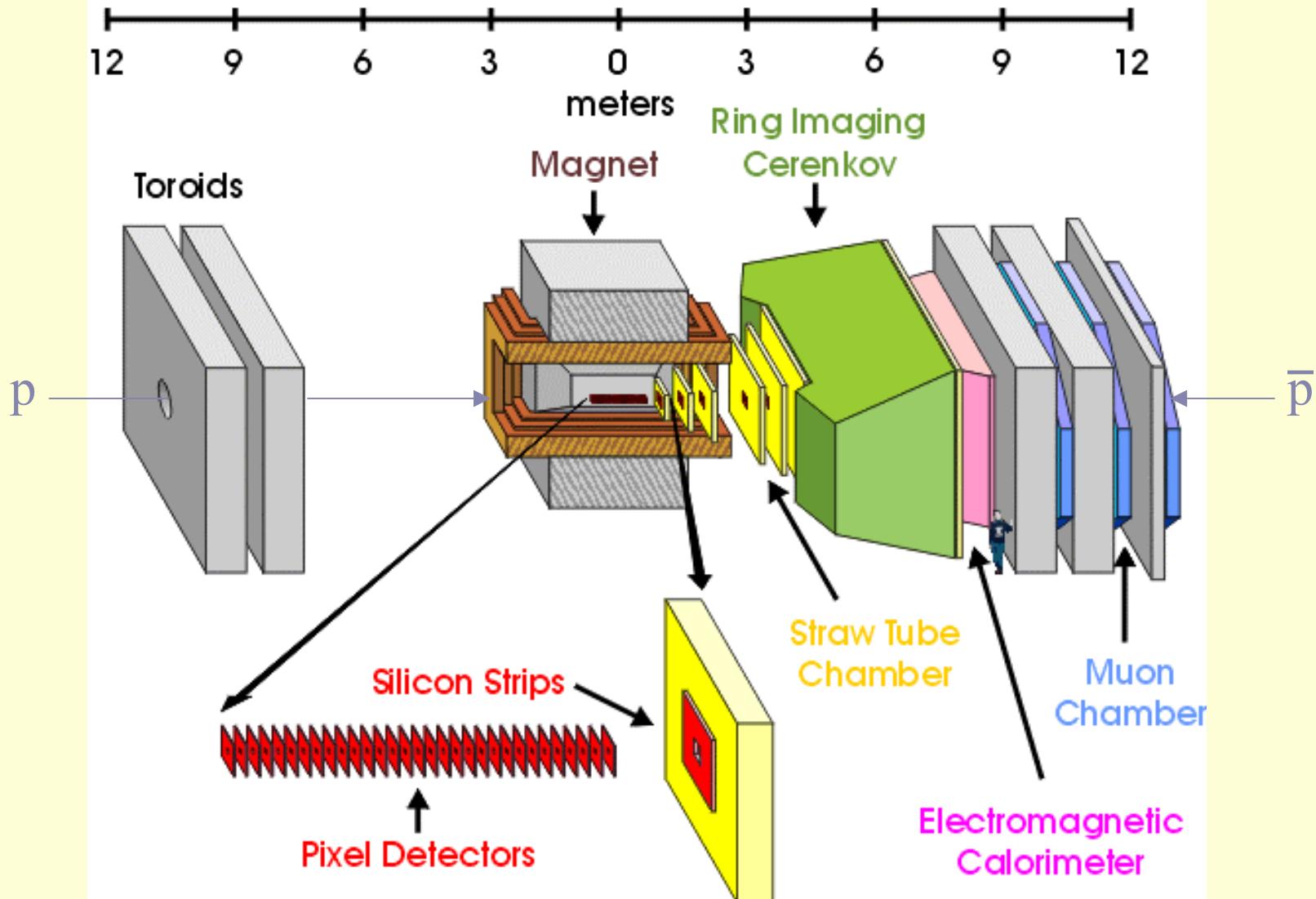
BTeV Pixel and FST System



Simon Kwan
Fermilab

Presentation at SIDET, November 3, 2003

BTeV Detector Layout



Pixel Detector WBS 1.2

Fermilab: J. A. Appel, D. C. Christian, S. Cihangir, J. Fast, R. Kutschke, S. Kwan, M. Marinelli, M. Wang, G. Cardoso, H. Cease, C. Gingu, J. Hoff, A. Mekkaoui, T. Tope, M. Turquetti, R. Yarema, J. Howell, C. Kendziora, C.M. Lei, A. Shenai, A. Toukhtarov, M.L. Wong , G. Lanfranco, D. Slimmer, D. Zhang, S. Austin, S.Jakubowski, R. Jones, G. Sellberg, M. Ruschman

Frascati: S. Bianco, F. Fabbri, M. Caponero

Iowa: C. Newsom, T. Nguyen, J. Morgan

Milano: G. Alimonti, S. Magni, D. Menasce, L. Moroni, D. Pedrini, S. Sala, L. Uplegger

Syracuse: M. Artuso, C. Boulahouache, J.C. Wang,

Tennessee T. Handler, R.Mitchell, S. Berridge

Wayne State: D. Cinabro, G. Bonvicini, A. Schriener, , A. Guiterrez, G. Gallay, S. LaPointe

Wisconsin: M. Sheaff

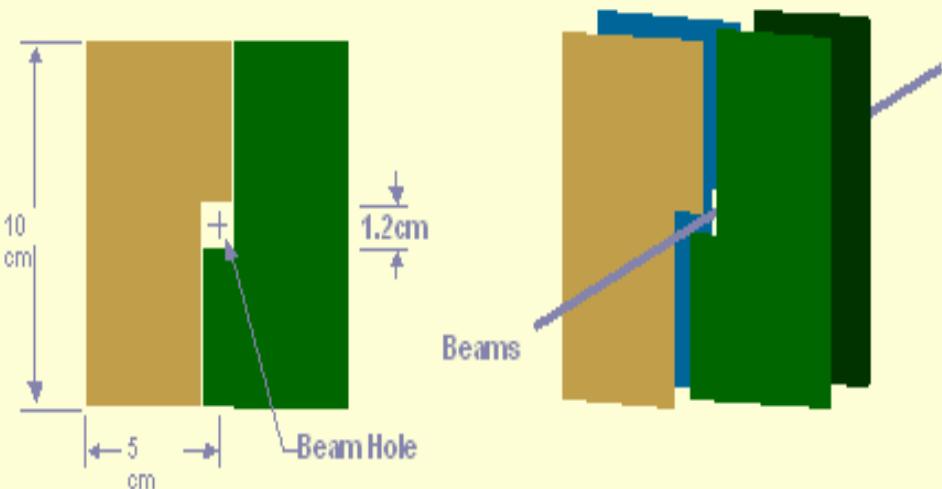
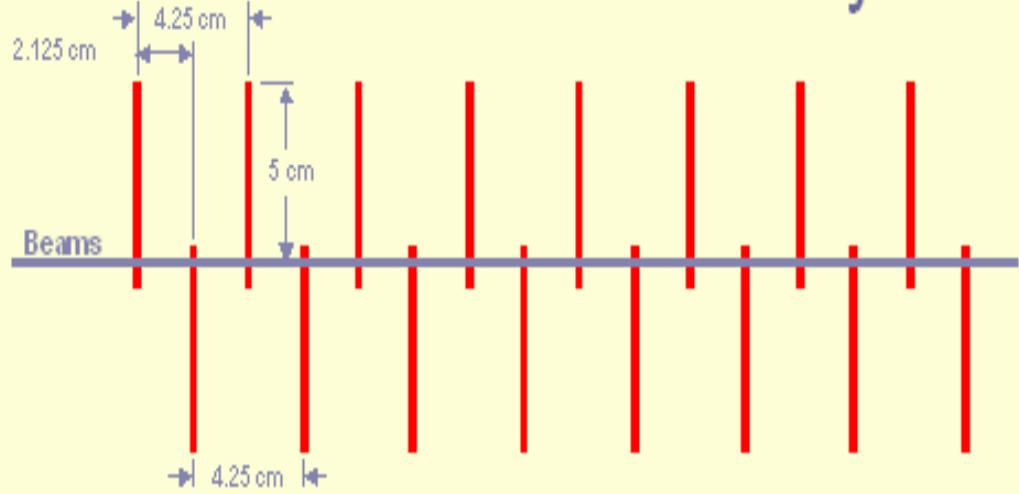
Pixel Vertex Detector

Reasons for Pixel Detector:

- Superior signal to noise
- Radiation Hard
- Excellent spatial resolution: <9 microns depending on angle, etc
- Pattern recognition power
- Very low occupancy

Special features:

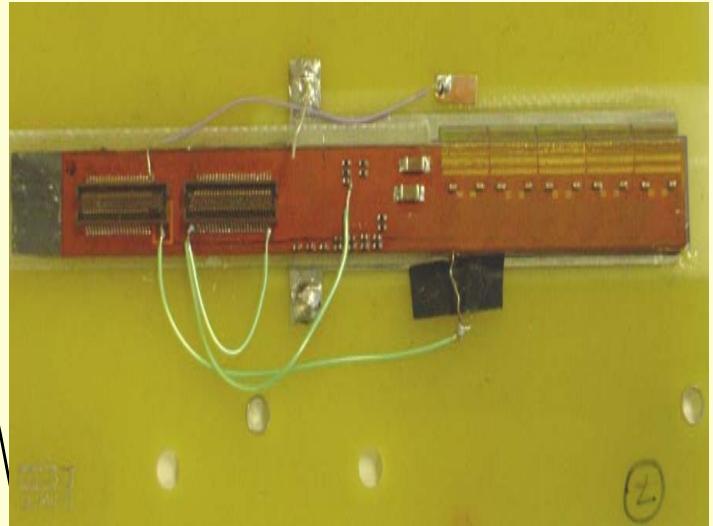
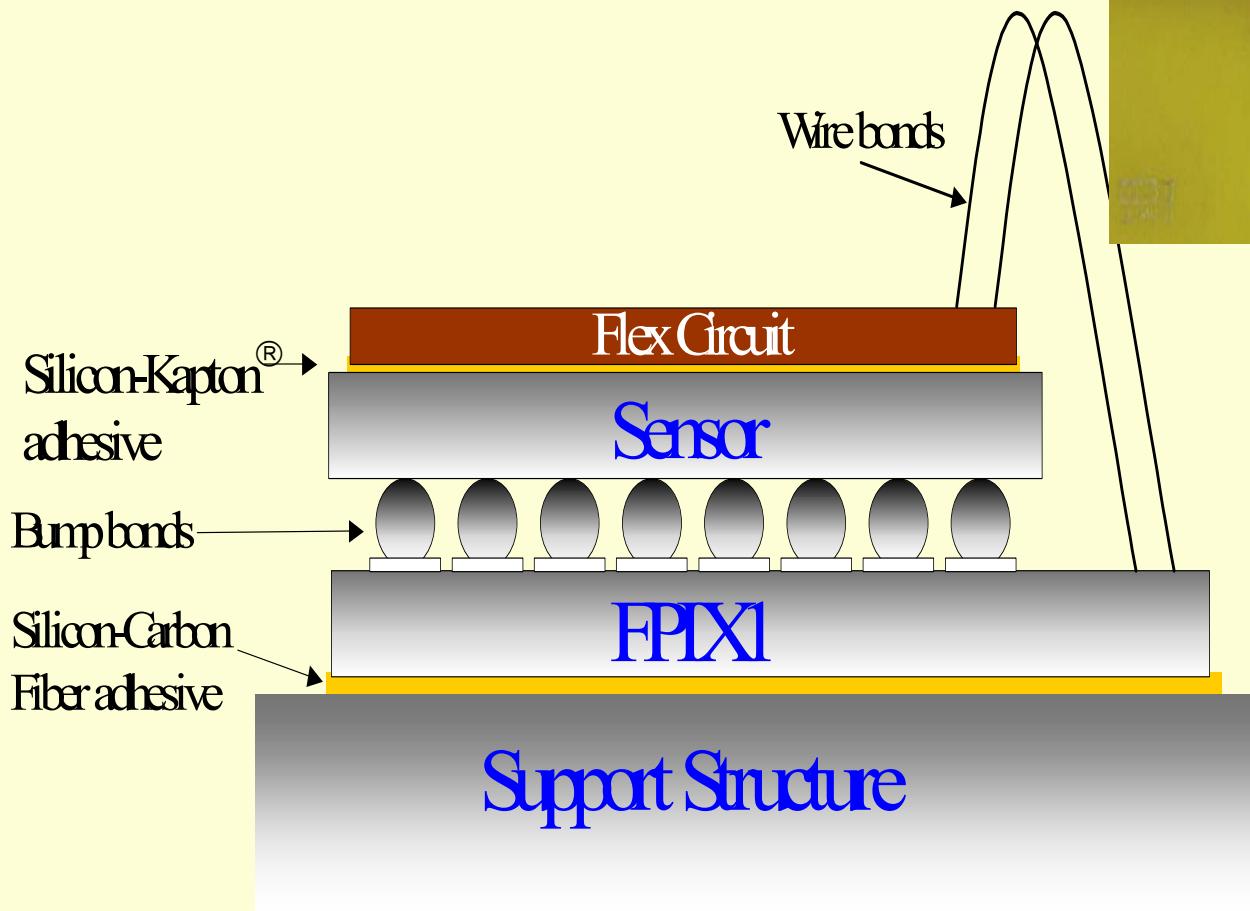
- Info used directly in the L1 trigger.
- Placed inside a dipole and gives a standalone momentum measurement.
- Sitting close to beam and in vacuum
- 30 stations and 23 million pixels in total
- Total length ~1.3m



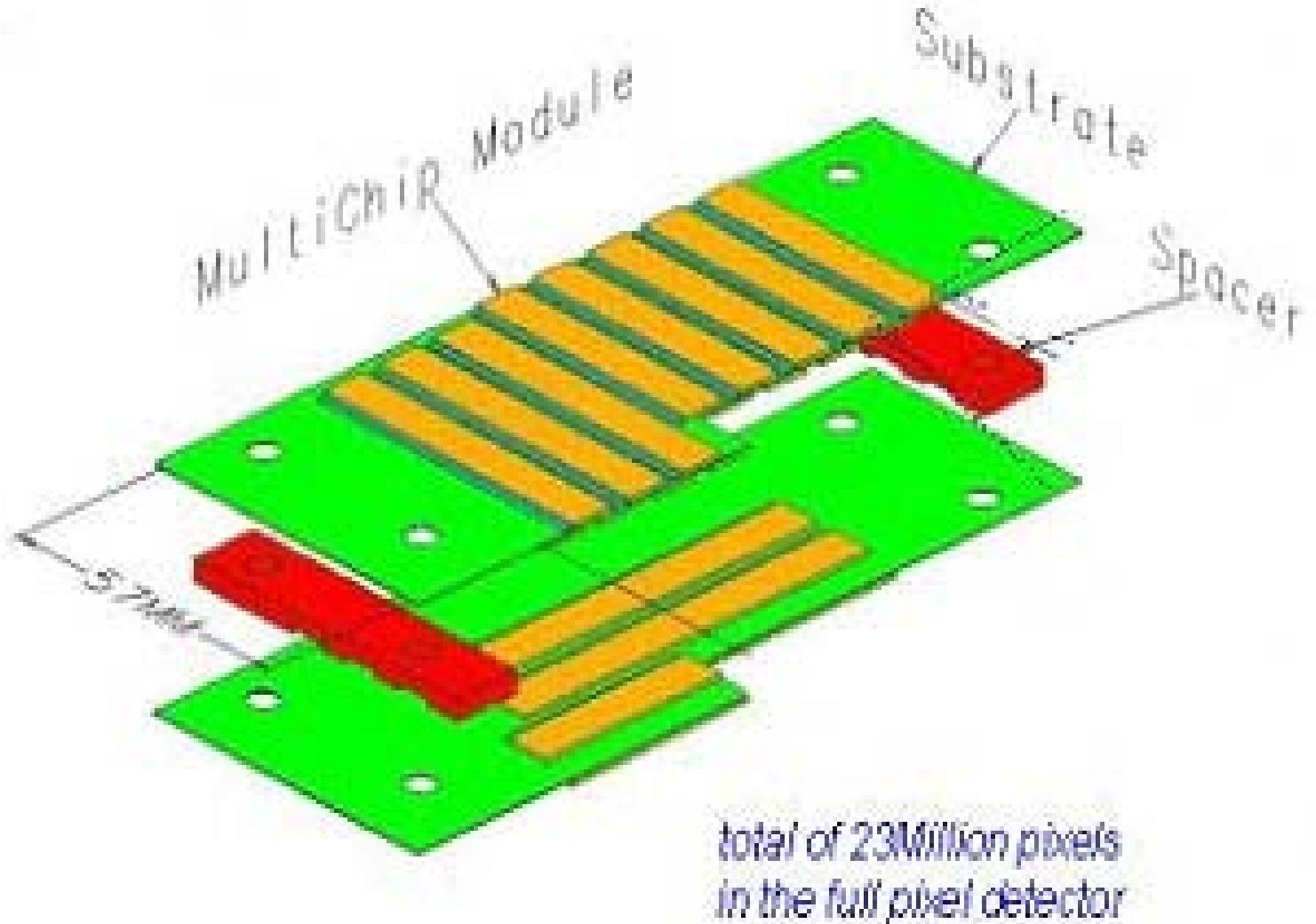
BTeV Pixel Vertex Detector Properties

Property	Value
Pixel Size	$50 \times 400 \mu\text{m}^2$
Outer plane dimension	10 cm x 10 cm
Central square hole (adjustable)	Nominal setting: 12mm x 12mm
Total number of planes	60
Total number of stations	30
Total number of pixels	23 million
Total Silicon active area	0.5 m ²
Separation of stations	4.25 cm
Pixel plane orientations (per station)	One with narrow pixel dimension vertical and the other with narrow dimension horizontal

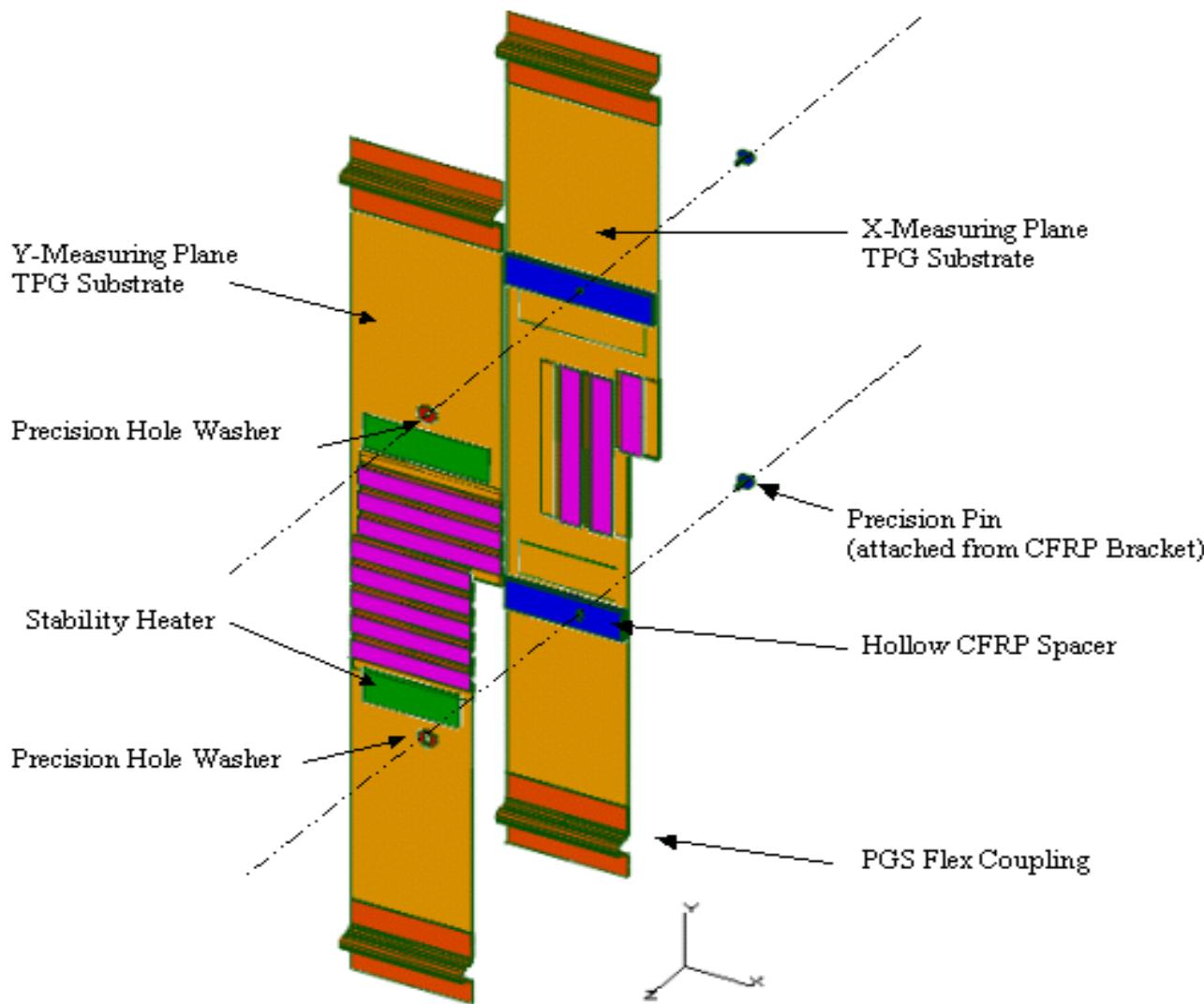
Pixel Detector

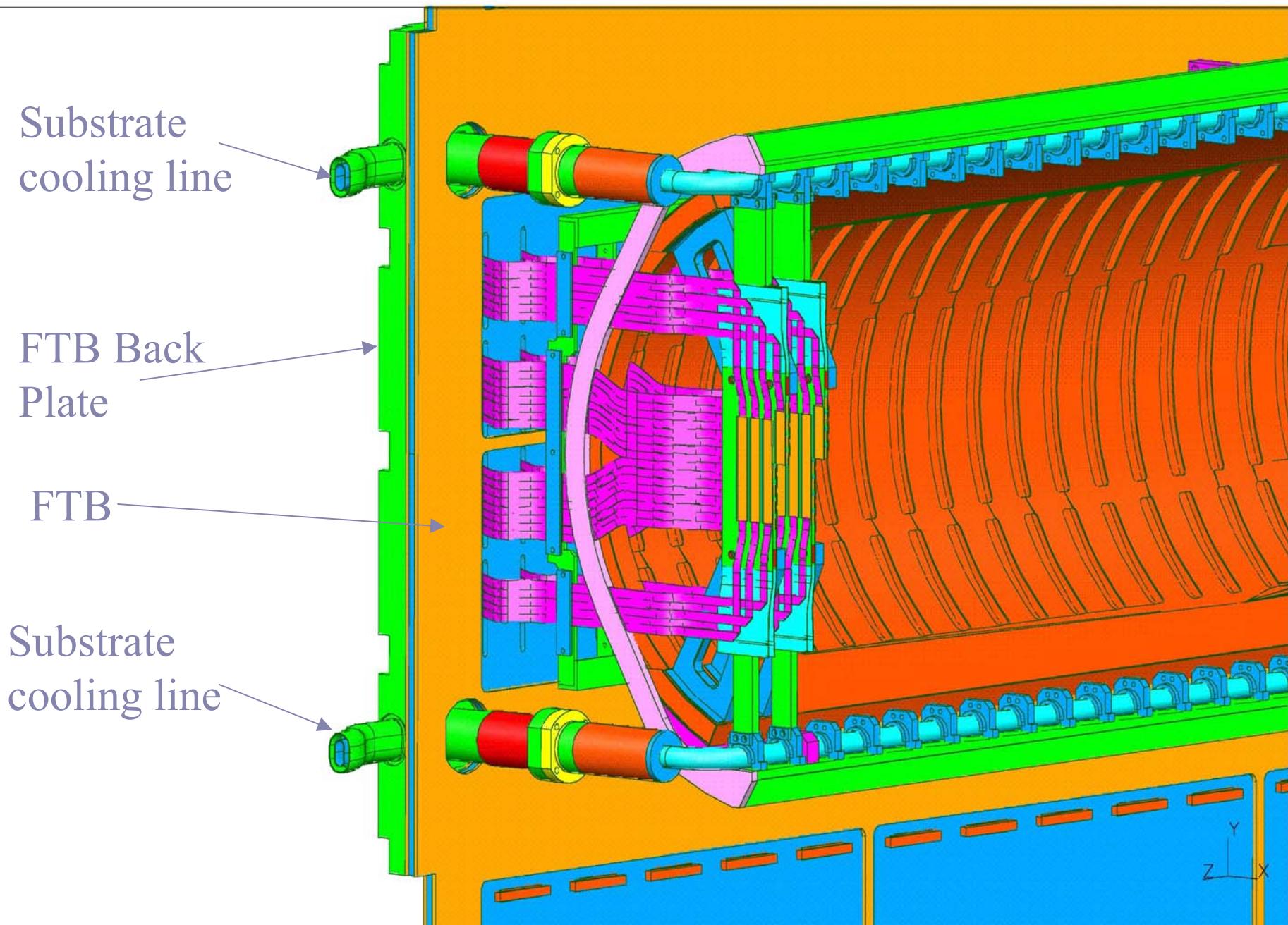


Multi-Chip Module

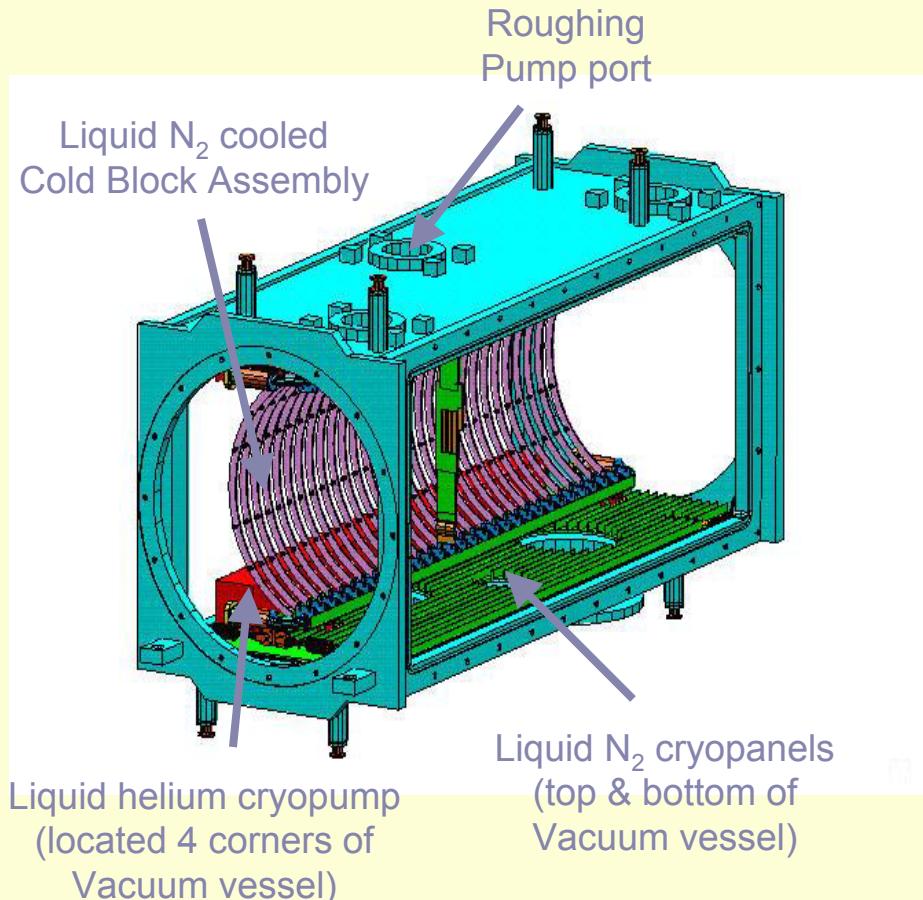


TPG Substrate





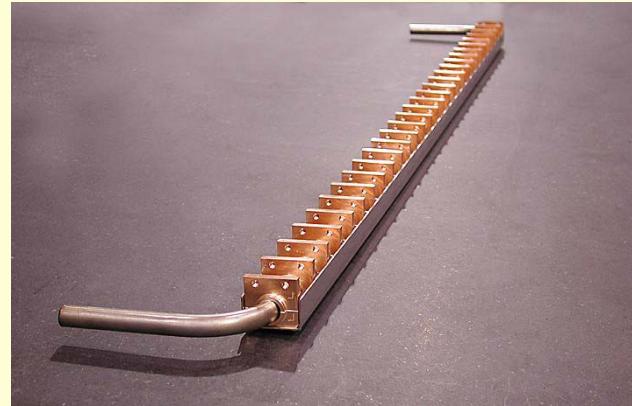
Conceptual Design for Vacuum System



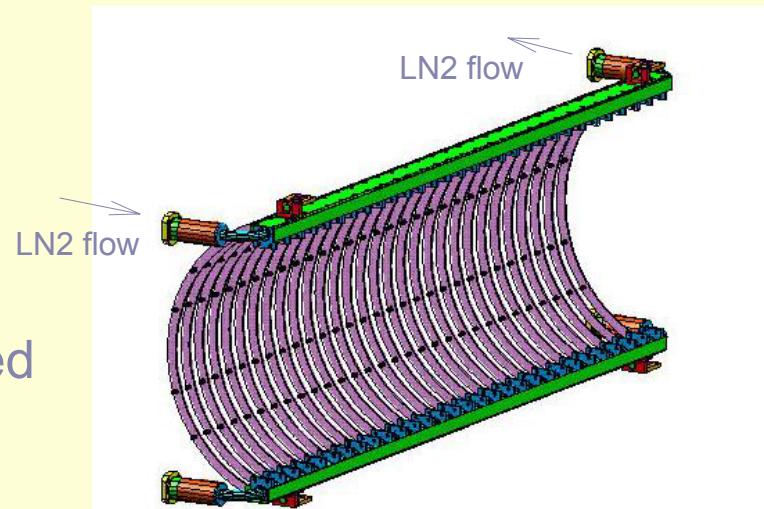
- Designed based on gas load measurement using a model with ~ 5% of detector components that contribute to outgassing
- Majority of gas load is water
- ~1% of gas load is N₂
- Huge water pumping capacity using cryopanels, cold block assembly and LN₂ thermal shield of the LHe cryo-pump
- LHe cryo-pump for non-condensable gases
- Expected pressure better than 1×10^{-7} torr

Pixel Detector Cooling

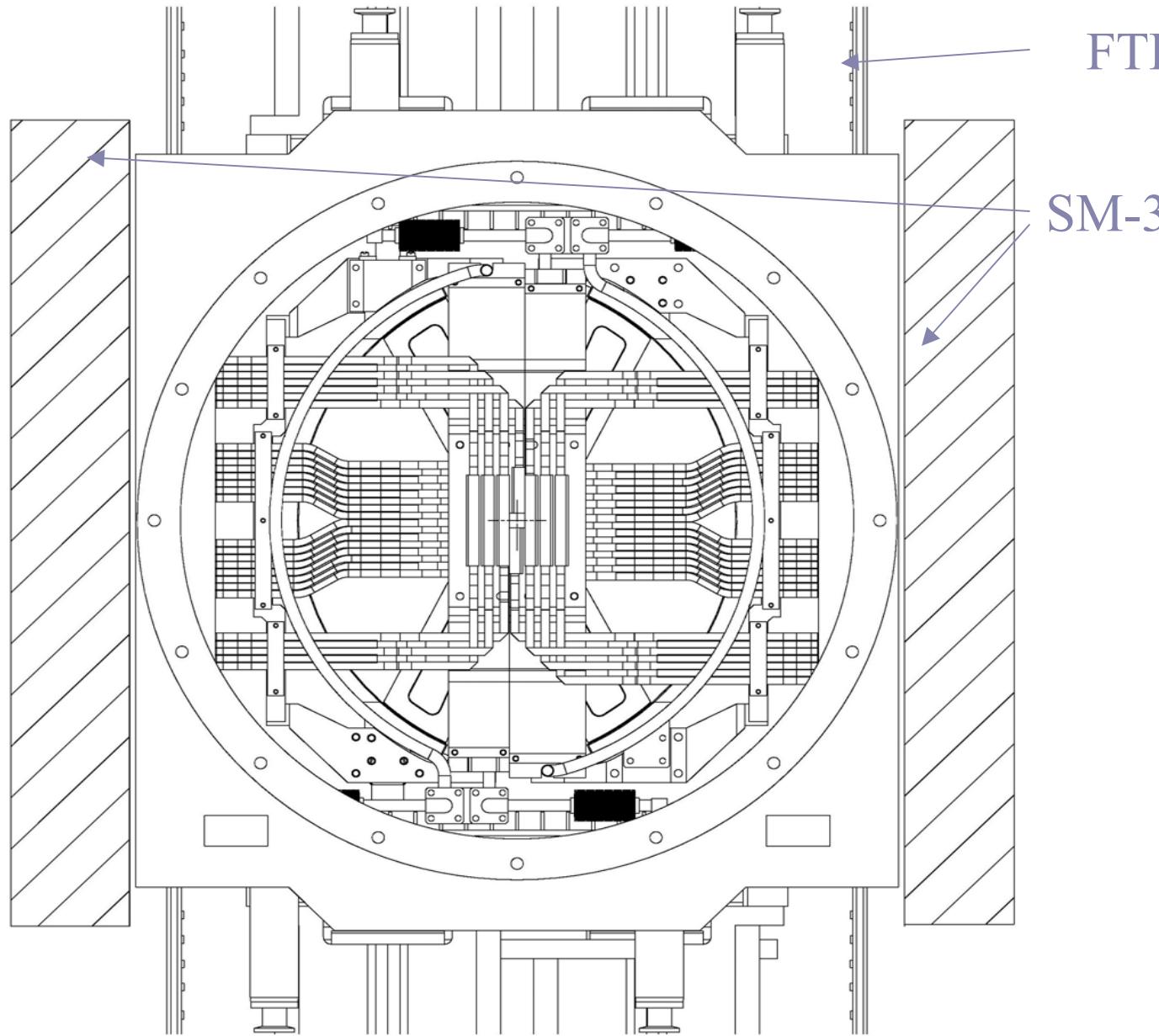
- **Cooling requirement:**
Maintain silicon sensor temperature around -5°C
- **Cooling System: Cold Block Assemblies and Aluminum Ribs**
- **Cold Block Assembly:**
 - Stainless steel LN_2 cooling lines
 - TPG connected to Cu blocks brazed to tube
 - Flow and vibration testing in process
 - No direct cooling fluid-to-Tevatron vacuum joints



Prototype Cold Block Assembly



**Cooling System for Half of a Detector,
Including 2 Cold Block Assemblies &
Thermal Conducting Aluminum Ribs**

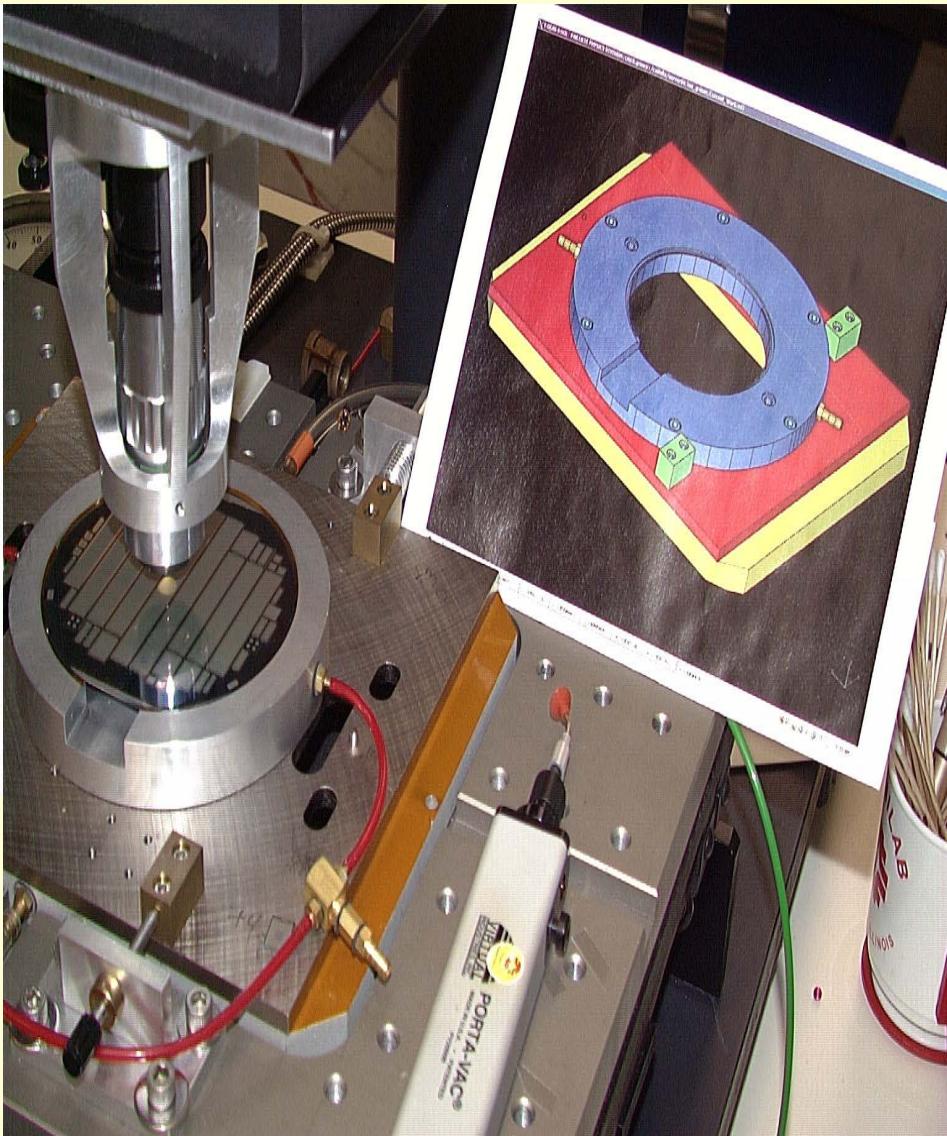
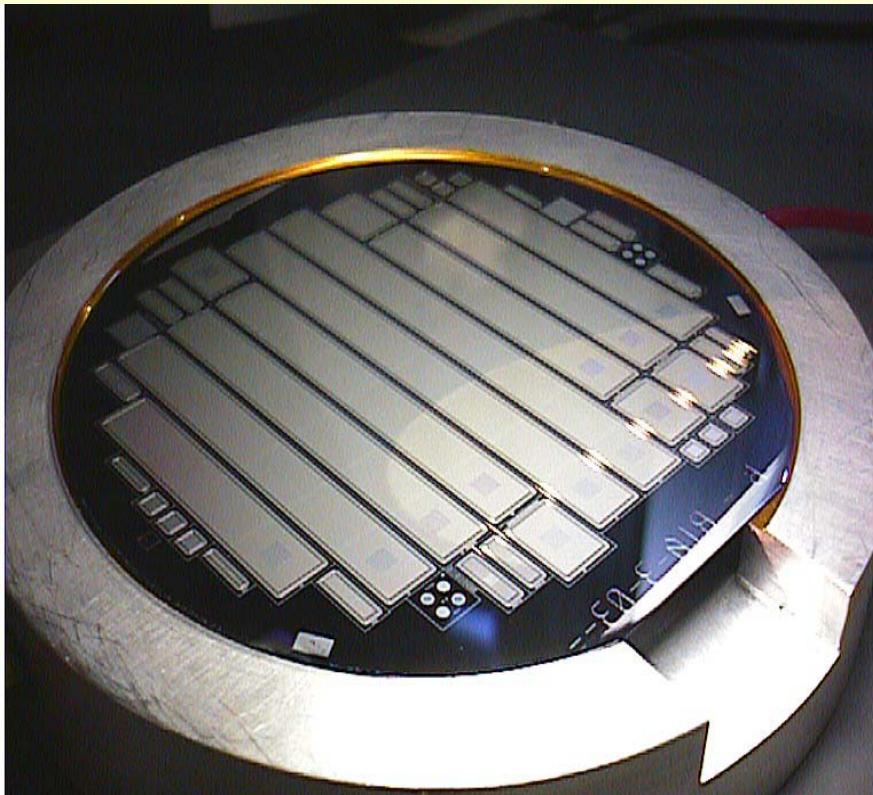


Detector Front View

Pixel R&D

- Effort started in 1997
- Ongoing activities at SIDET, FCC, Village (Labs 3,5,6,8), PAB, WH14, MTEST
- Also at collaborating institutes
- Lab A: sensors, bump bonding studies, module placement, flex cable tests
- Test area: Laser test station, magnet, PGS flexing test, irradiated sensor tests
- Lotima room: TPG studies, mock-up

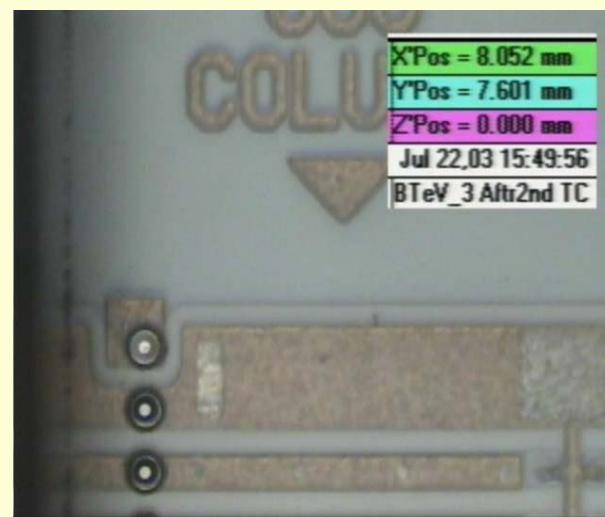
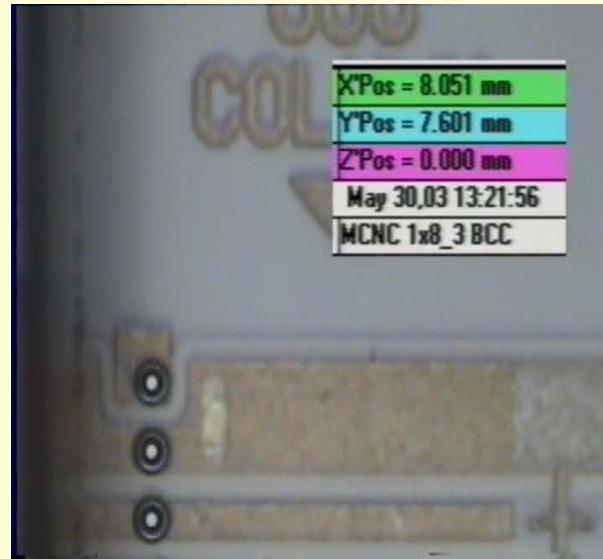
BTeV TESLA Wafers



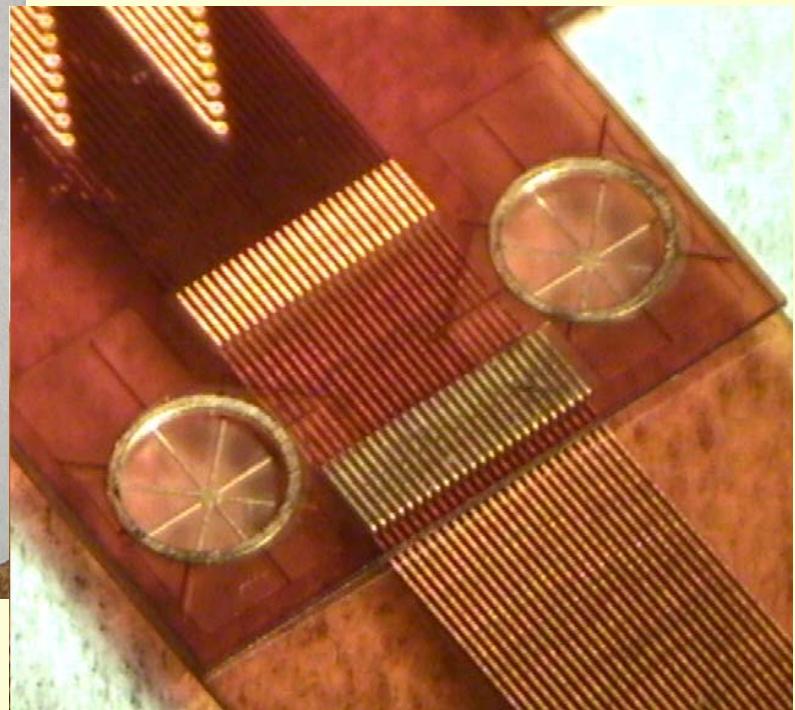
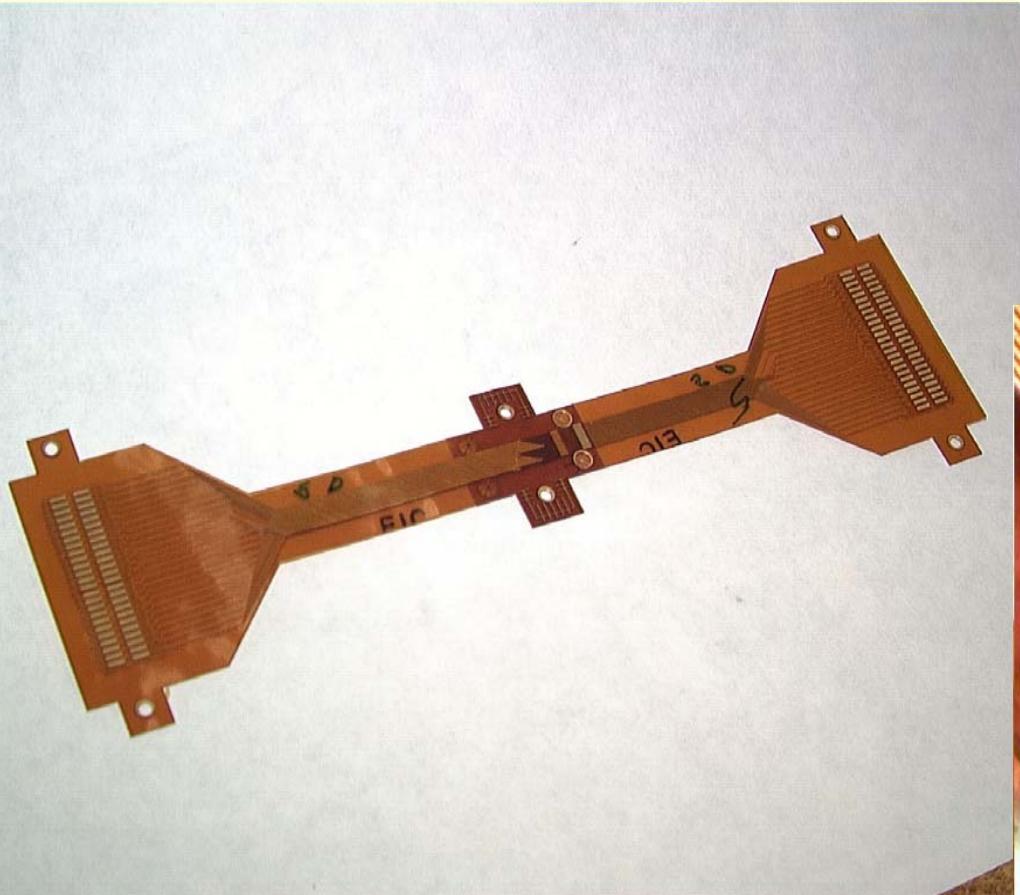
- 1 “4-chip” module
- 3 “6-chip” modules
- 3 “5-chip” modules
- 2 “8-chip” modules
- 5 “1-chip” sensor

Bump bonding

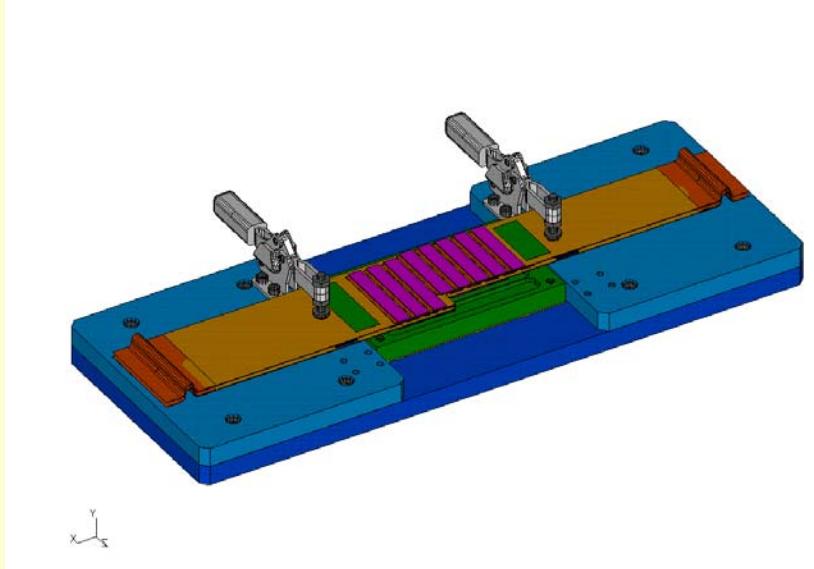
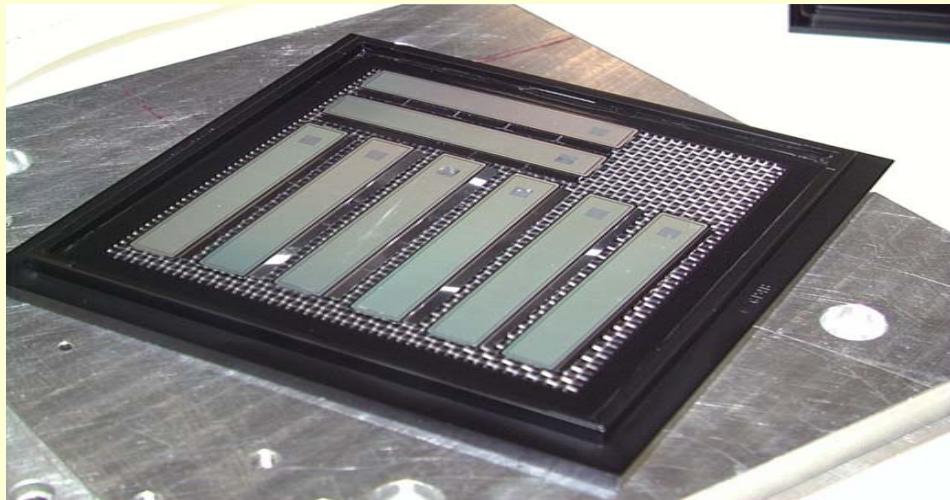
- Concern: yield, reliability, effects due to thermal cycling, attachment to substrate (CTE mismatch)
- Bump bonding studies
 - thermal cycle studies on glass-Si modules
 - Thermal cycle studies on detectors
 - Radiation effects
 - CTE mismatch effects

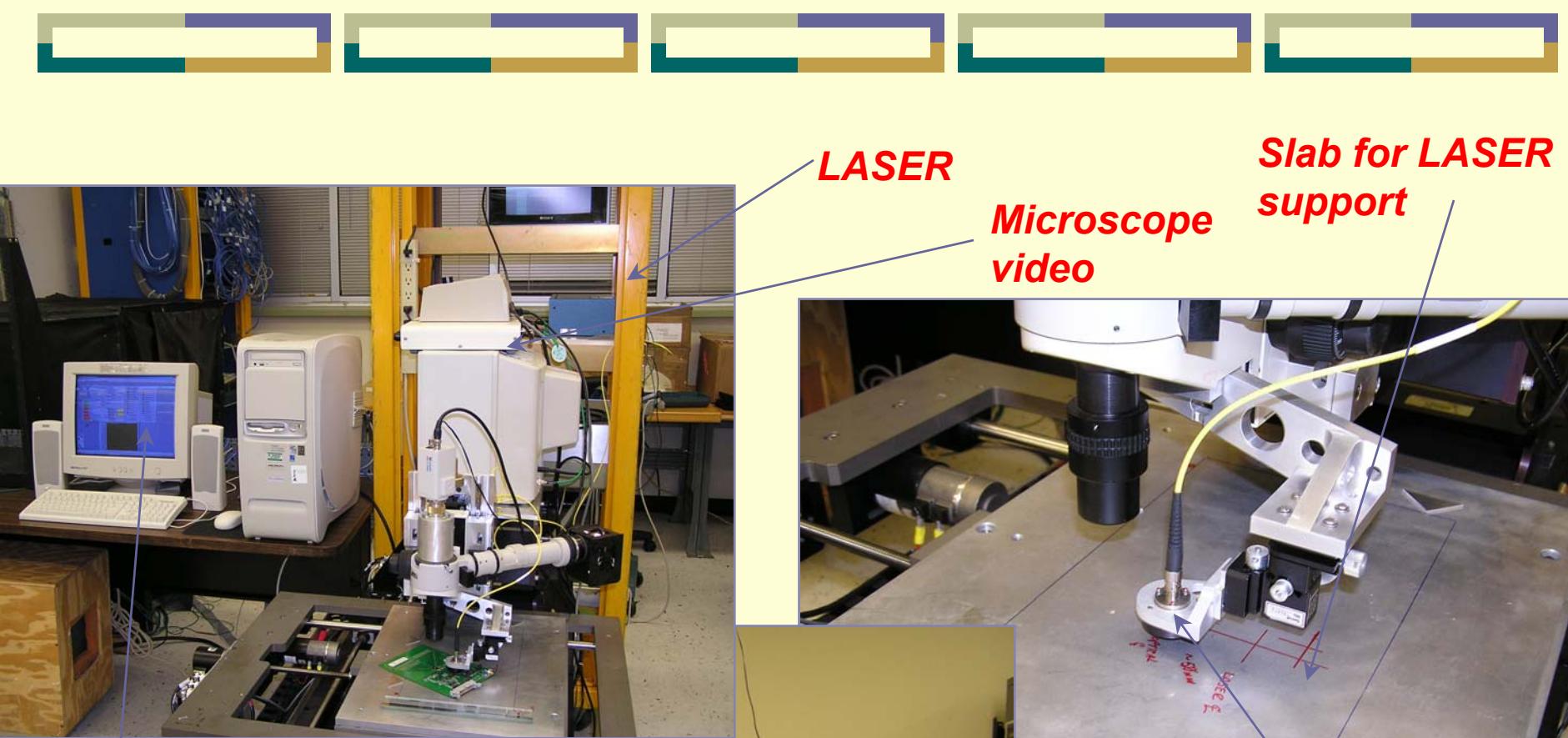


Pixel Interconnect Flex Cable



Module Assembly on TPG





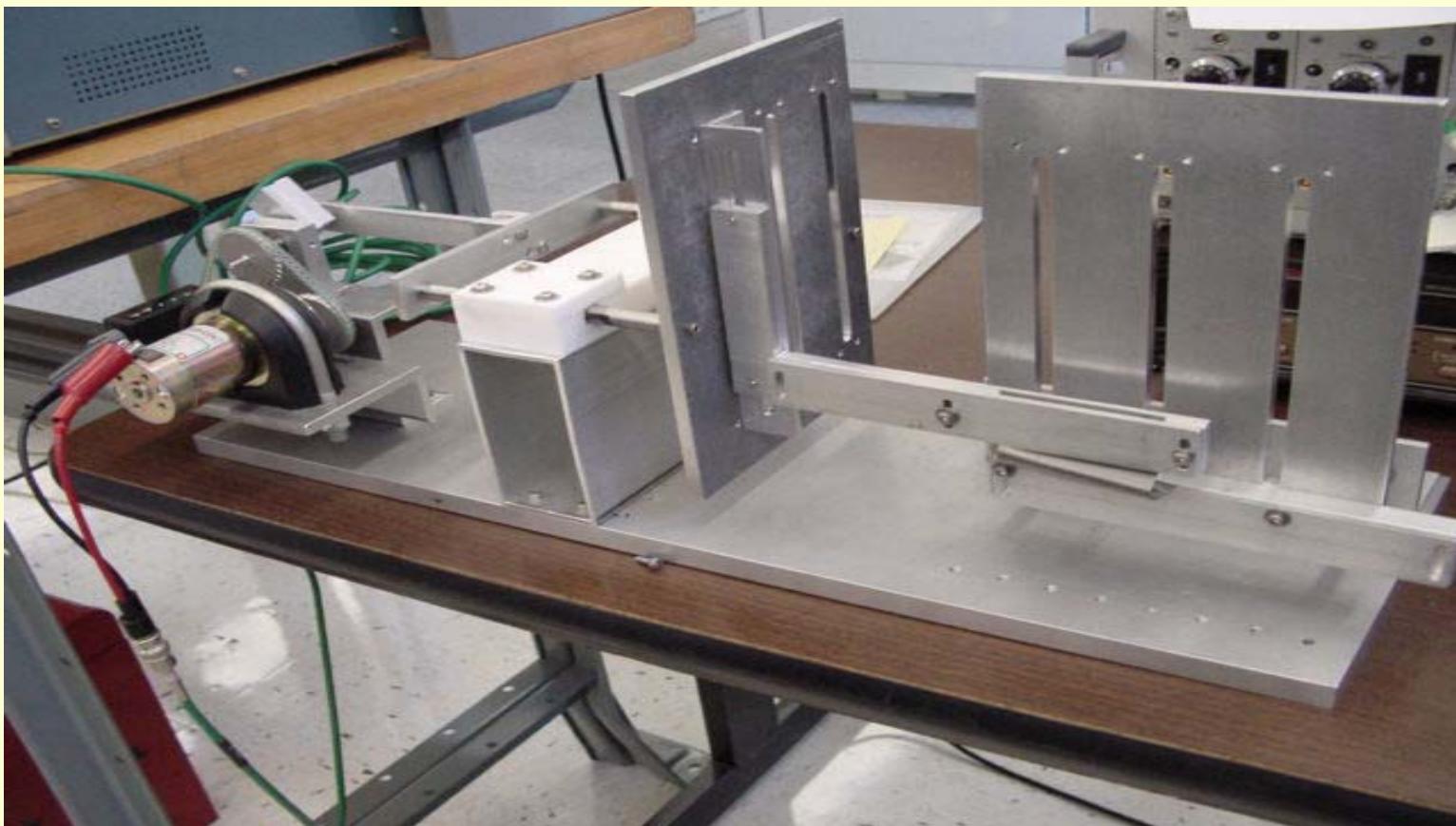
**Software
for the
detector
remote
control &
positioning**



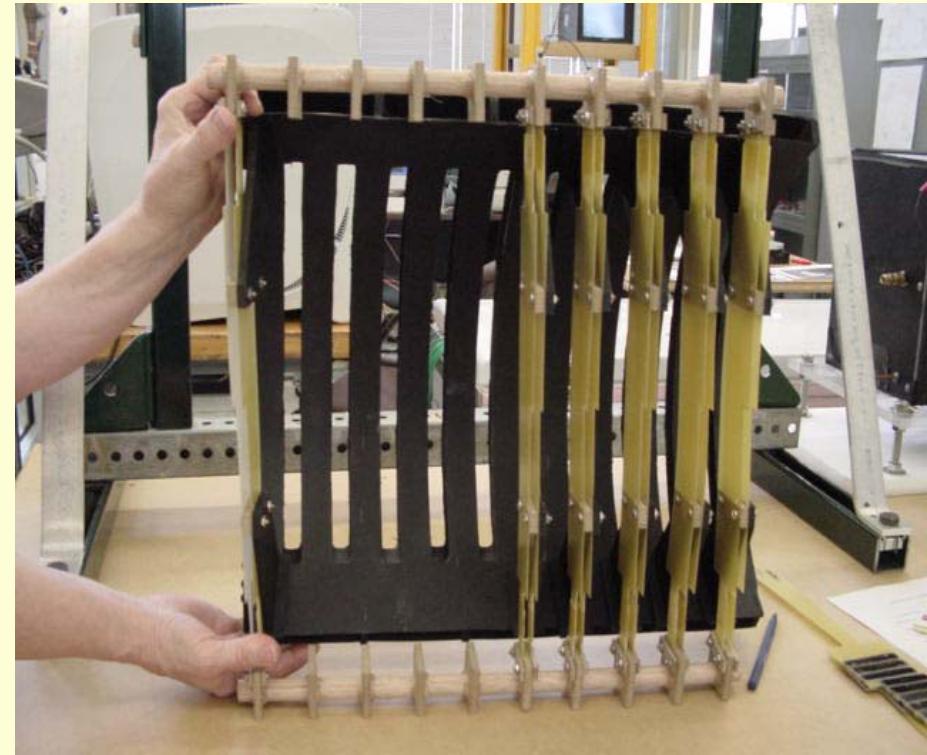
**Microscope
for the
alignment**

**LASER
optics**

PGS flexing



Carbon Support Structure

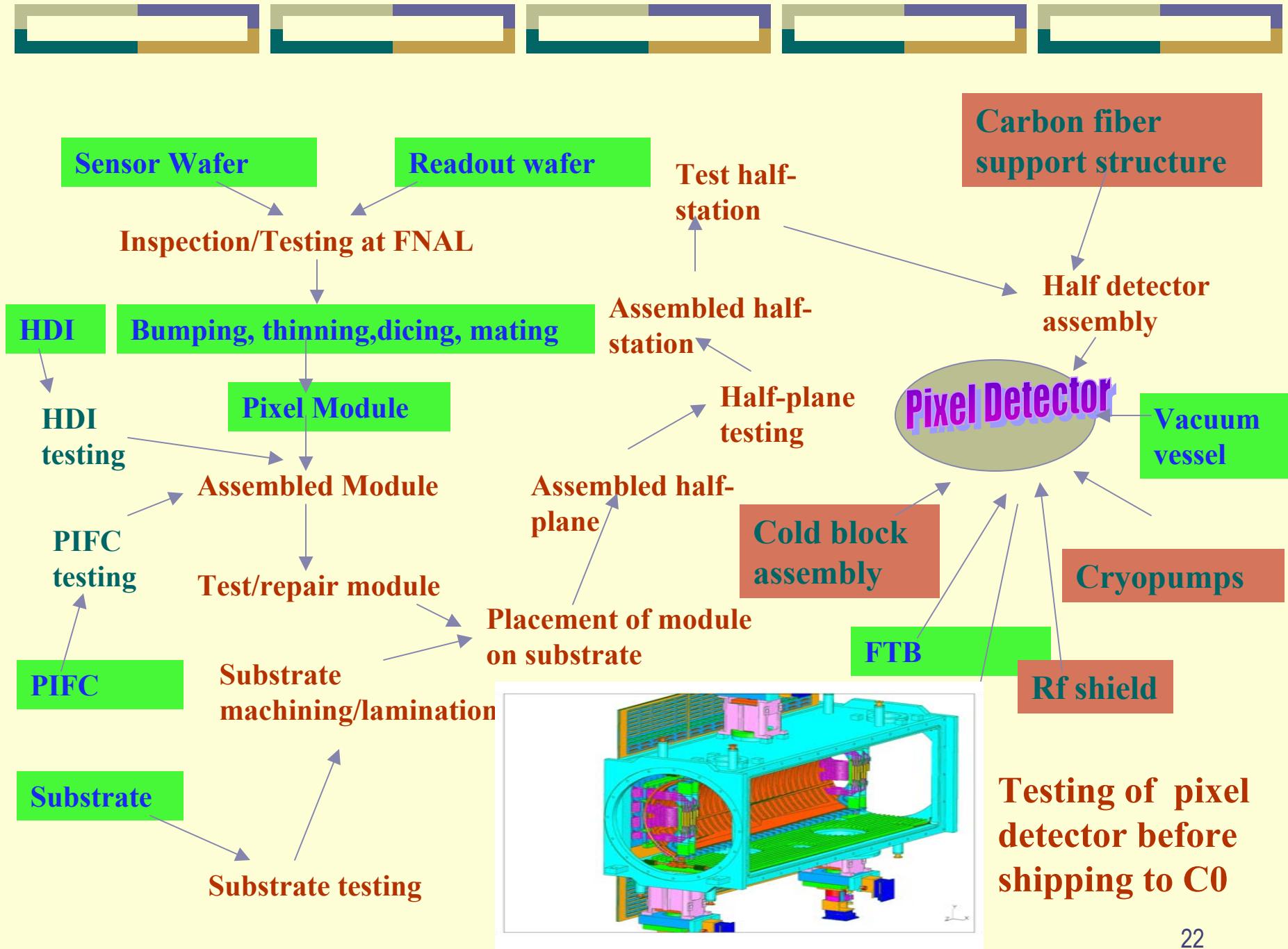


- 1st prototype tested in Lab C
- 2nd prototype ready next month
- Will be tested in Lab C again for deflection and thermal stress
- Frascati group will bring FBG/ESPI tools to do tests here

Mock-up to understand cable routing issues; needs a bit of work to complete the model

Components

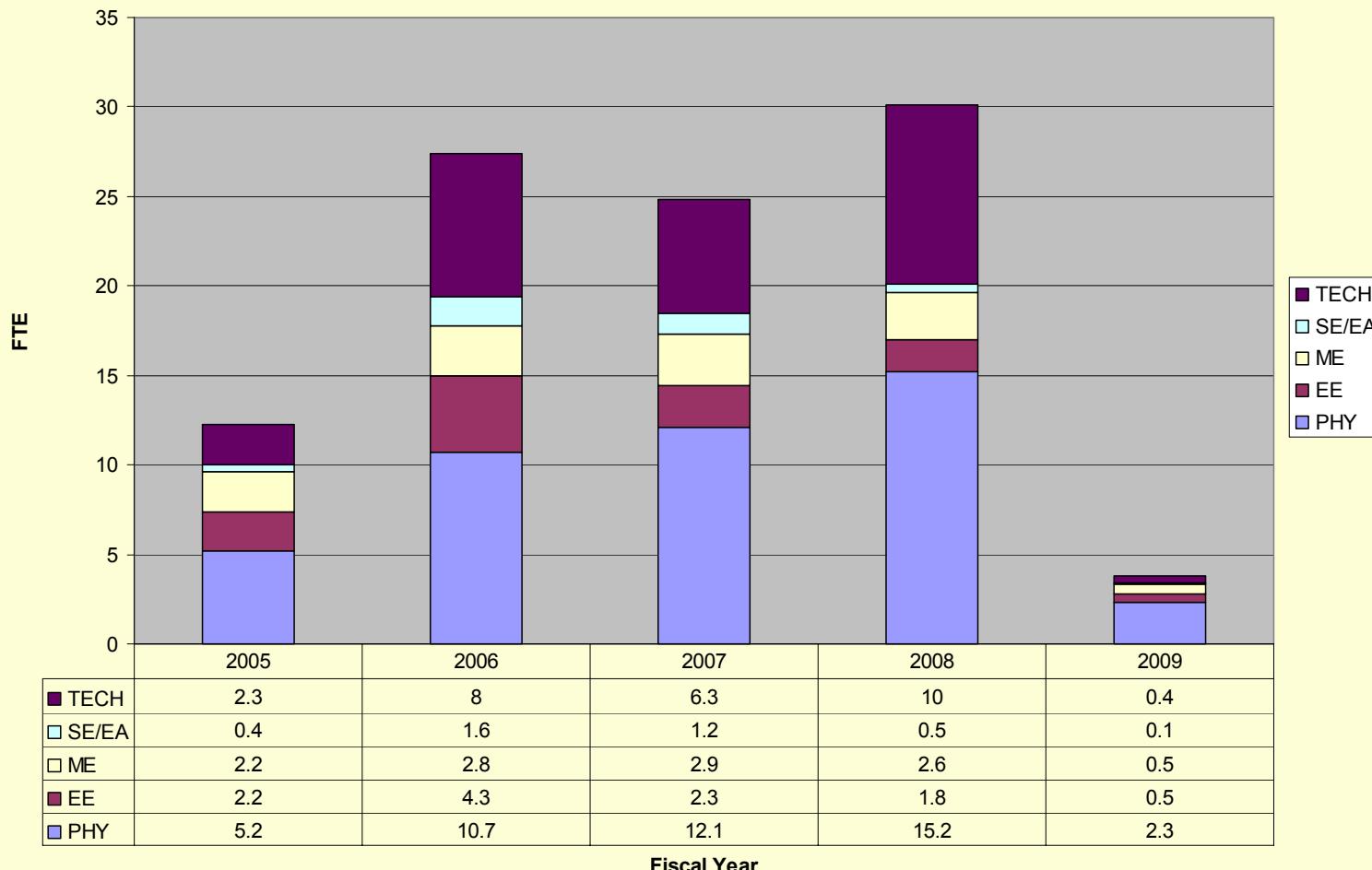
Items	Quantities		Prototype iterations	Status
	Base	Additional		
Working Readout chips	8100	2700	4	Ready for pre-production
Working Sensor modules	1380	520	2	Test beam studies, ready for preproduction
HDI	1680	520	2	Design for new modules
PIFC set (power and data)	1680	520	1	Full prototype testing
Bumping (ROC wafers)	50	15	4	Thinning study, working with new vendors
Bumping (sensor wafers)	200	60	4	New TESLA wafer
Flip-chip assembly	1380	520	4	Moderate scale module assembly; 50 in total
Wire bonds	567K	189K		
Stations	30		1	1 complete half-station
TPG Substrates	120	40	2	Prototypes testing
C support structure	2	2	2	New prototype
Cryo pumps	2		1	Technical design
Secondary Pumps (cryopanel)	1 lot		1	Technical design and prototype testing
Actuators	8	0	2	New prototype
Cooling system	1 lot	0	1	Prototype testing
Data cable	780	160	1	Prototype testing
LV Power and sensing cable	240	48		
HV Power cable	1380	280		
HV channels	1380	144	1	Test prototype
LV channels	2760	288	1	Test prototype
Vacuum vessel	1			Complete design
Rf shield	1 lot		1	EMI study, finish design and interact with BD
Feedthrough board	12	4	2	Prototype (PO pending)
PDCB	120	20	0	Design



Timeline

- FY 04: last year of RD project
 - Modest increase in our effort at SIDET
- DOE baseline review: summer '04
- Construction project starting FY05 – 09
 - **3% system assembly/test: FY05/06 ?**
 - Preproduction : starting mid- FY05
 - **10% system assembly and test at C0: FY07/FY08**
 - Production: starting late FY06
 - **Detector ready for installation: Q1/FY09**

WBS1.2 Pixel Personnel Usage per FY

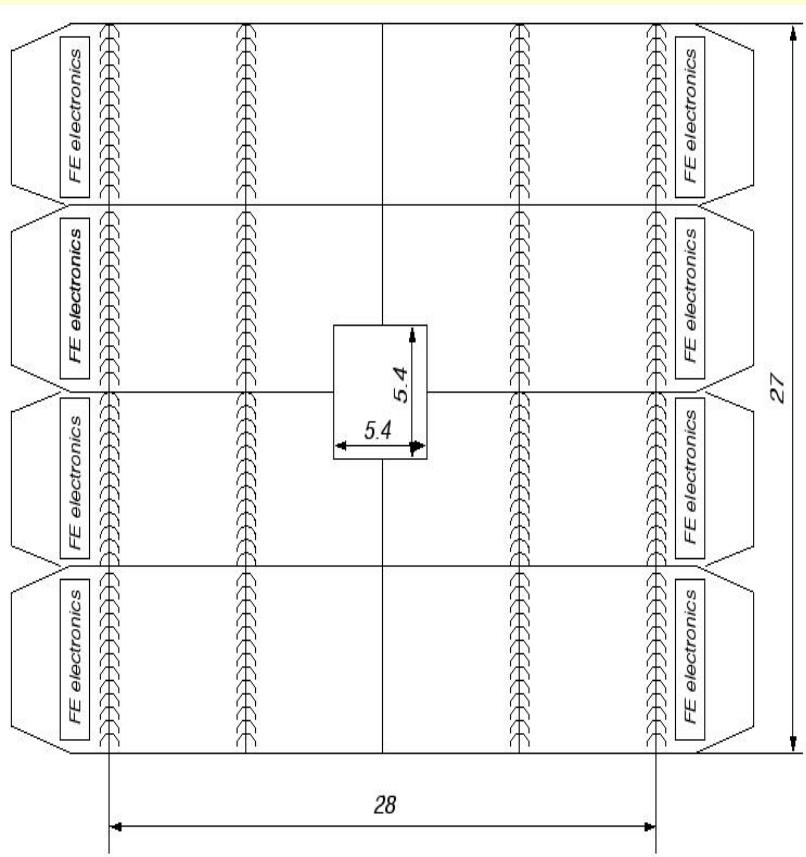


Forward Silicon Tracker WBS 1.7

- **Colorado University:** J.Cumalat, P.Rankin, Eric Erdos
- **Fermilab:** J. Fast, G. Cardoso, C. Gingu, J. Hoff, A. Mekkaoui, R. Yarema, J. Andresen, K. Knickerbocker, A. Dyer, H. Cease, D. Olis
- **Insubria University:** P. Ratcliffe, M. Rovere
- **INFN Milano:** G. Alimonti, M. Citterio, S. Magni, D. Menasce, L. Moroni, D. Pedrini, S. Sala, S. Erba, L. Uplegger, P. D'Angelo, S. Latorre, M. Malatesta
- **INFN Pavia:** G.E. Cossali, P.F. Manfredi, M. Manghisoni, M. Marengo, L. Ratti, V. Re, M. Santini, V. Speziali , D. Di Pietro, G. Traversi , K. Fisher, L. D'Angelo

Baseline Silicon Tracker Design

- 7 stations
 - 3 in dipole fringe field
 - 3 before RICH
 - 1 after RICH
- Coverage from beam pipe to $\pm 13.5\text{cm}$ from the beam
- Each station has 3 planes of $300\ \mu\text{m}$ thick SMD with $100\ \mu\text{m}$ pitch
- Each detector is $7\times 7\text{ cm}^2$

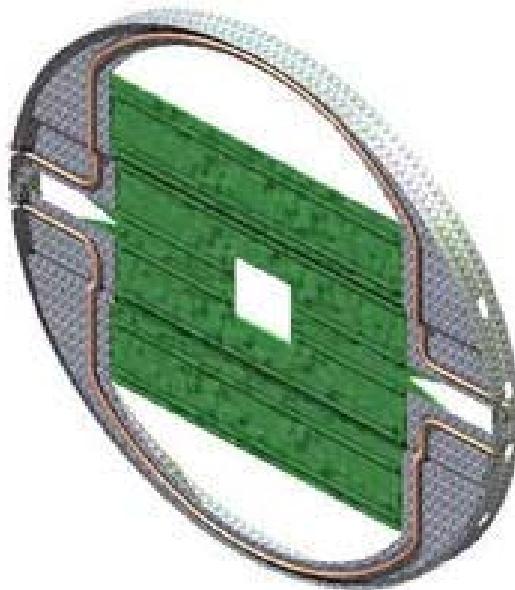


Si Tracker:General Properties

Property	Value
Silicon Sensors	$\sim 7 \times 7\text{cm}^2$, <i>p-on-n</i> type
Pitch	$100\mu\text{m}$
Thickness	$300\mu\text{m}$
Sensor configuration	4 ladders with 4 sensors each
Coverage	$27 \times 27\text{cm}^2$
Central Hole	$5.4 \times 5.4\text{cm}^2$ ($7 \times 7\text{cm}^2$ for last station)
Total Stations	7
Z Positions	85.5, 127.5, 185.5, 277.5, 321.5, 371.5, 714.5
Views per Station	3 (X,U,V)
Channels per view	$\sim 5,600$
Total Channels	$\sim 127,600$
Readout	Sparsified Binary

Silicon Tracker Mechanical Support & Cooling

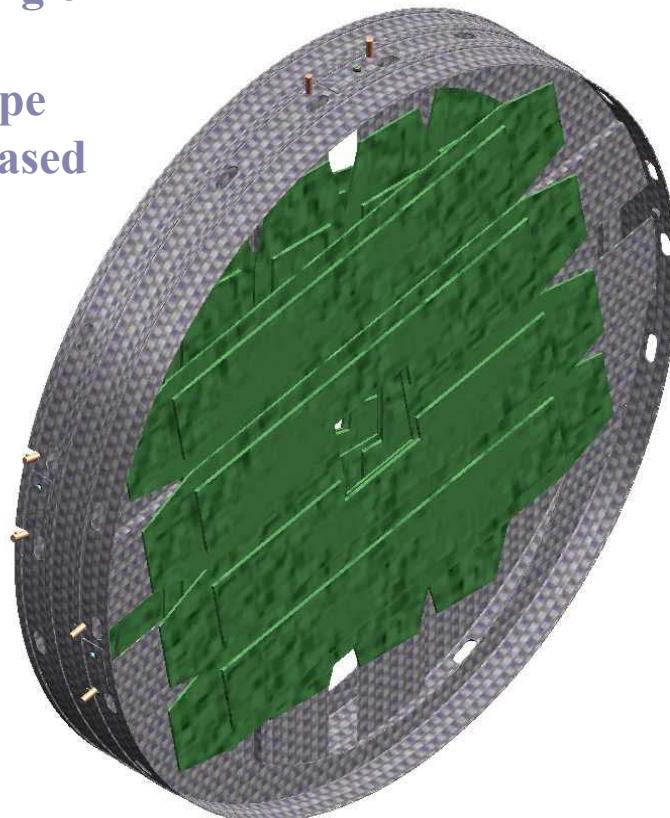
- Light weight carbon frame holding the 4 ladders forming the plane
- Opening along a diameter allow wrapping around beam pipe
- Cooling ducts on backside



Forward Silicon Strip Station Assembly

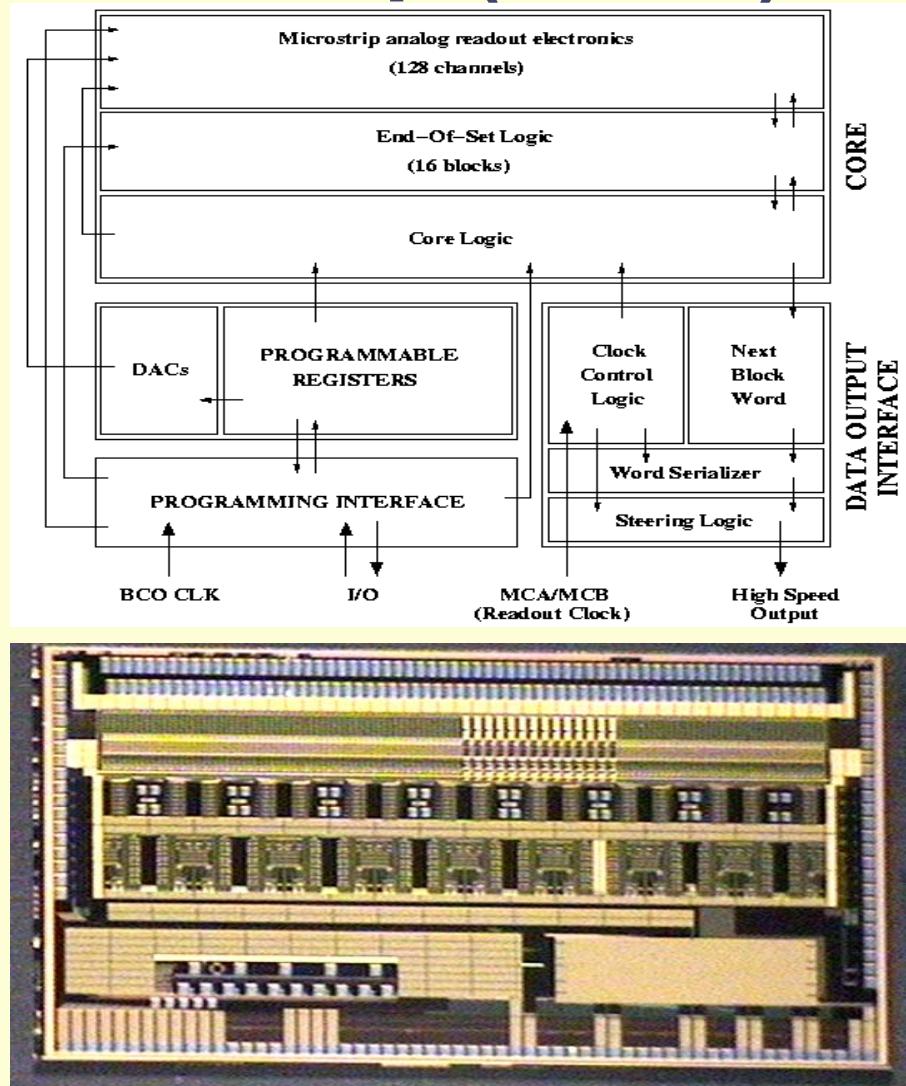
Forward Silicon Strip Tracker: crucial to cover the small angle region near the beam. The straw detector could not cope with the high occupancy. Based on three views with $100\mu\text{m}$ Strips.

3 views can be stacked to form a station. Reference pins guarantee a very precise relative alignment.

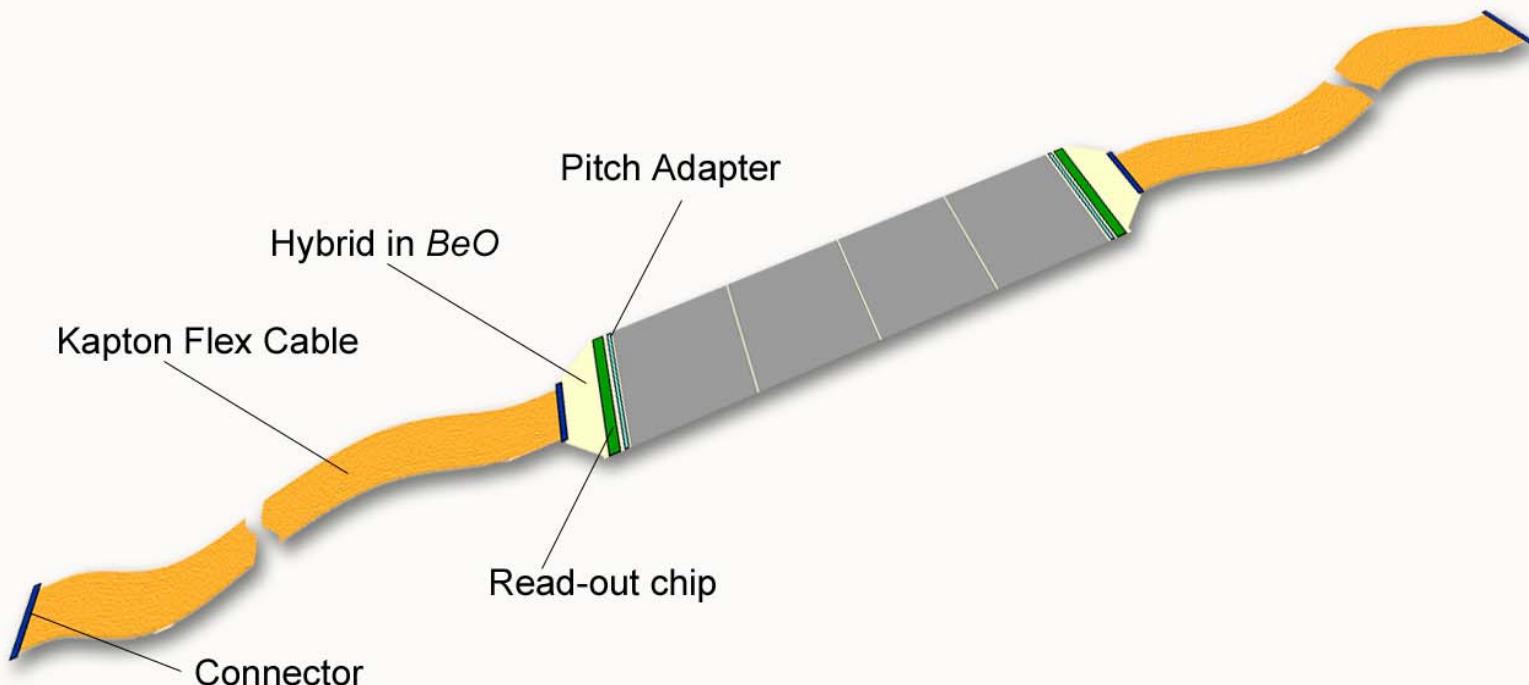


Silicon Strip Readout Chip (FSSR)

- Temple 2002: The one area, which appears to have the most technical risk, is the readout chip.
.... the silicon readout chip is still to be designed.
- Use 0.25 μm CMOS
- Collaboration between Pavia & FNAL
- Fast and data-driven readout (large bandwidth)
- 4 logic sections
- Architecture identical to FPIX pixel ROC
- 128 channels arranged into 16 sets of 8 strips
- 40 prototype chips delivered

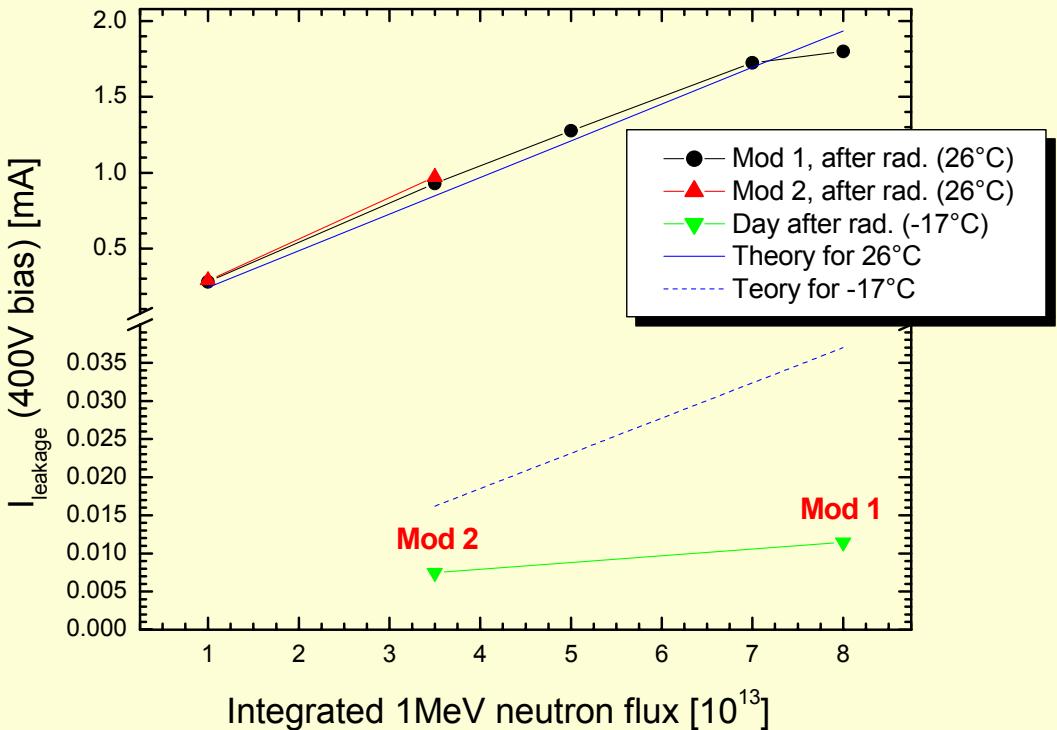


Ladder Configuration



I_{leak} -irradiation Dose Curves

Leakage current vs. irradiation fluency



Theoretical model (ROSE collaboration)

- Detectors are currently stored at -17°C @ IUCF
- Will bring them to the lab in 2 weeks time
- Test using laser test stand
- Need work on cold chuck, dark box etc

BTeV FST at SIDET

- This sub-system will get substantial funding and support from INFN (Italy)
- Some work started here to help to get the project ready for DOE review
- Fermilab will have a major role in hybrid, flex cable development, and the readout chip
- Possibility of final assembly done at SIDET
- We will help in the Mechanical support and cooling system design
- Detail plan/schedule will be developed over the next few months